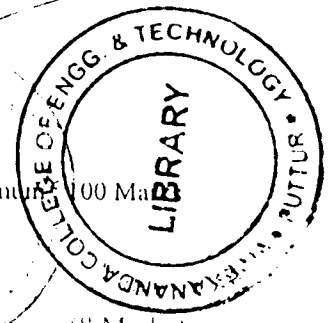


Fourth Semester BE (CSE/ISE)
COMPUTER ORGANIZATION - CSE46
MODEL QUESTION PAPER

Time : Three Hours

Maximum 100 Marks

Answer any five full questions.
All questions carry equal marks.



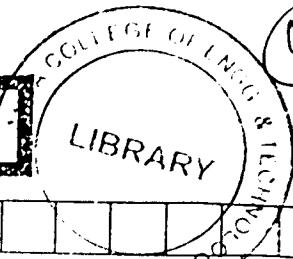
1. a) List the steps needed to execute the machine instruction ADD LOC, R0 in terms of transfers between the components of processor & memory. Assume that the instruction itself is stored in the memory location INSTR. (8 Marks)
- b) Explain how the performance of the computer can be measured. (6 Marks)
- c) Explain the following (6 Marks)
 - i) Byte addressability
 - ii) Big-endian assignment
 - iii) Little-endian assignment
- 2 a) Register R5 is used in a program to point to the top of the stack. Write a sequence of instructions using the index, auto increment and auto decrement addressing modes to perform each of the following tasks (12 Marks)
 - i) pop the top two items of the stack, add them and then push the result onto the stack
 - ii) copy the fifth item from the top into register R3
 - iii) remove the top ten items from the stack
- b) Consider the following possibilities for saving the return address of a subroutine: (8 Marks)
 - i) In a processor register
 - ii) In a memory location associated with the call, so that a different location is used when the subroutine is called from different places.
 - iii) On a stackWhich of these possibilities supports subroutine nesting and which supports subroutine recursion?
3. a) Three devices, A, B, and C, are connected to the bus of a computer. I/O transfers for all three devices use interrupt control. Interrupt nesting for devices A and B is not allowed, but interrupt request from C may be accepted while either A or B is being serviced. Suggest different ways in which this can be accomplished in each of the following cases. (6 Marks)
 - i) The computer has one interrupt-request line.
 - ii) Two interrupt-request line, INTR1 and INTR2, are available, with INTR1 having higher priority.

Specify when and how interrupts are enabled and disabled in each case.

- b) Explain DMA. (10 Marks)
- c) What is bus arbitration? Explain two methods of bus arbitration. (8 Marks)
4. a) Explain synchronous DRAM with a neat diagram (10 Marks)
- b) What is a cache? Explain any two cache mapping functions. (10 Marks)
5. a) Explain carry-lookahead adder. Write the number of gate delays required to perform n bit addition using ripple-carry adder and carry-lookahead adder. (10 Marks)
- b) Explain Booth's algorithm. Multiply two numbers -13(multiplicand) and 11(multiplier) using normal and Booth's multiplication method. (10 Marks)
6. a) With a neat diagram explain floating point addition/subtraction unit. (10 Marks)
- b) With a neat diagram explain the hardwired control unit (10 Marks)
7. a) Explain 3-bus organization of the data path with a neat diagram and write the control sequence for the instruction ADD R4, R5, R6 for the 3-bus organization. (10 Marks)
- b) Write a flowchart of a microprogram for the instruction - Add src, Rdst. (10 Marks)
8. Write Short notes on (4 X5 = 20Marks)
- a) Embedded system
- b) Assembler directives
- c) ROMs
- d) SCSI bus

6. (a) Explain general rules for floating point. (9 Marks)
- (b) Explain the non restoring division algorithm. Using this algorithm calculate quotient and remainder, considering dividend, divisor as 1000 and 0011 respectively. (6 Marks)
- (c) Explain causes for pipeline stall. (10 Marks)
7. (a) How instruction pipelining increases performance of system? Explain this idea with 4-stage pipeline. (5 Marks)
- (b) Compare RISC and CISC processor. (5 Marks)
- (c) Explain magnetic disk principle and organization of data on disk. (5 Marks)
8. Write short notes on the following : (4 x 5 = 20 Marks)
- a) Array processor
 - b) Bus and Ring topology in Law.
 - c) FAST Adder Circuits
 - d) Register structure in 8086.

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NEW SCHEME

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Page No... 1

Fourth Semester B.E. Degree Examination, July/August 2004

**BM/EC/IT/TE/ML/EE/CS/IS
Computer Organisation**

Time: 3 hrs.]

[Max.Marks : 100

**Note: 1. Answer FIVE Questions.
2. All questions carry equal marks.**

1. (a) Consider the memory system of a computer storing the following data :

Address in Hex	Data stored (binary)
2000	00111000
2001	00110100
2002	00110010
2003	00111001

Interpret the storage as numbers in the manner indicated below and find their decimal values in each case.

- Big-endian storage of 2 hex words of 4 - digits each
- Big-endian storage of 2 BCD words of 4 - digits each.
- Little - endian storage, in ASCII, of a 4 - digit signed hex word.
- Little endian storage, in ASCII, of a 4 - digit BCD word. (2 × 4 = 10 Marks)

(b) Give reasons to justify using, generally,

- Single address instructions in 8 - bit CPU's
- Double address instruction in 16-bit CPU's
- Three address instructions in RISC systems

In each of these systems give assembly language programs for performing the operation :

data at mem A + data at mem B → memC.

(10 Marks)

2. (a) What do you understand by stack frames ? Discuss their use in sub-routines. (10 Marks)

(b) Write an assembly program to multiply 2 memory arrays and store their result in a third memory array :

$a(i) \times b(i) = c(i)$ for $i = 0$ to $n - 1$.

Consider load/store and 3-address system.

(10 Marks)

3. (a) Explain how interrupt request from several I/O devices can be communicated to a processor through a single INTR line.

(b) Which type of I/O devices are interfaced through DMA ?

Explain the bus arbitration process used for DMA.

(10 Marks)

4. (a) Explain the general features of interfacing a parallel I/O port to a processor. (10 Marks)

(b)

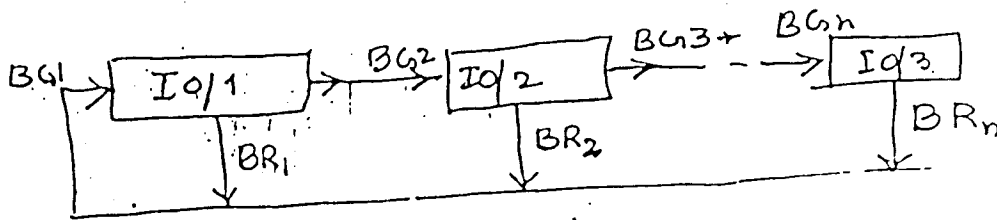


Fig Q 4 b)

Consider the daisy chain arrangement shown in fig Q.4b in which the bus request signal from the I/O is directly fed back as bus grant signal. Assume device IO/3 requests the bus and begins using it. When the device is finished, it deactivates BR3. Assume the delay from BG_i to BG_{i+1} in any device is d . Show that a spurious bus-grant pulse will travel down stream from device 3. Estimate the width of this pulse. (10 Marks)

5. (a) Describe SDRAM and DDR SDRAM operations for data transfer between main memory and cache memory systems. (10 Marks)

(b) Consider a processor running a program 30% of the instructions of which require a memory read or write operation if the cache hit ratio is 0.95 for instructions and 0.9 for data. When a cache hit occurs for instruction or for data, only one clock is needed while the cache miss penalty is 17 clocks to read/write on the main memory. Work out the time saved by using the cache, given the total number of instructions executed is 1 million. (10 Marks)

6. (a) Work out the multi level look - ahead carry scheme for doing a 32 bit number addition. How many gate delays are required to do the complete addition in this method? (10 Marks)

(b) The hexa decimal value of π is 3.243F6A8885A308D3... Work out the IEEE standard representation (IEEE standard 754-1985) of π in single and double precision formats. (5+5 Marks)

7. (a) Show the basic organisation of a CPU in terms of registers and other units for a single bus data path CPU. In such a CPU, show the complete action of the CPU in fetching and executing the instruction. (10 Marks)

Load R_1 from memory data at A, where A is a memory address. Assume the instruction is in one process or word. Indicate the control signals to be used at each stage of execution. (10 Marks)

(b) Explain the basic concept of micro programmed control. (10 Marks)

8. (a) With a block diagram explain the general requirements of a microwave oven OR a digital camera. (10 Marks)

(b) Write short notes on any TWO.

- i) A good method of hardware multiplication
- ii) SCSI bus
- iii) Virtual memory

7. (a) Show the control sequences for execution of Add (R3), R1 and explain. (6 Marks)
- (b) Explain the IEEE standards for floating point number. (8 Marks)
- (c) With block diagram, explain the working of microwave oven in an embedded system. (6 Marks)
8. Write short notes on : (5 × 4=20 Marks)
- i) Microprogrammed V/s hardwired control
 - ii) Virtual memory
 - iii) SCSI bus
 - iv) Multiprocessors and multi computers.

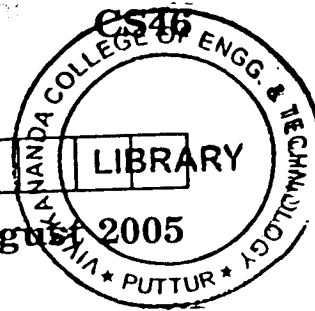
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NEW SCHEME

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LIBRARY



Fourth Semester B.E. Degree Examination, July/August 2005
Common to BM/EC/EE/TE/ML/IT/CS/IS
Computer Organisation

Time: 3 hrs.]

[Max.Marks : 100

Note: Answer any FIVE full questions.
All questions carry equal marks.

1. (a) Discuss the various generations through which the computers have evolved to the present stage. Indicate the important technological features and devices that characterised each generation. (10 Marks)
 - (b) Distinguish between unsigned and signed integers. With examples, indicate when each type of integers will be useful. (4 Marks)
 - (c) An integer of 32 bit size is stored in memory location in the little endian fashion. Indicate using a pseudo program, how a big endian 16-bit processor could rearrange the number and store it properly for its use, back in the same location. (6 Marks)
2. (a) Using register transfer notation, and concept of indirect addressing of memory, show how you can rearrange an ascending sorted data array to a descending sorted array in the same memory locations. Assume the array elements are of 16-bit size, and the processor system is also 16 bit size. (10 Marks)
 - (b) Consider the following :
 - i) A subroutine may require the parameters passed to it (from the main program), in a random order and more than once.
 - ii) A stack is a data structure in memory, from which the data can be accessed in a LIFO order and obviously a stack is not a suitable data structure for handling subroutine parameters.
 - iii) Yet, passing subroutine parameters through stack is perhaps the commonest way of handling subroutine parameters.

What mechanism is employed so that the parameters are made randomly accessible to the subroutine from the stack? Explain with an example. (10 Marks)
3. Show a circuit arrangement, whereby several devices may interrupt a processor on a single interrupt request line.
- If it is required to handle the device interrupts on a fixed priority basis, indicate in detail
- (i) A hardware based method
 - (ii) A software based method for addressing this requirement. (10 Marks)
- Explain the hardware registers that are required in a DMA controller chip. Why is it necessary for a DMA controller to be able to interrupt the processor? Explain. (10 Marks)

Contd... 2

4. (a) Explain the significant features of any ONE of the following bases :
i) PCI ii) SCSI iii) USB. (10 Marks)
- (b) Discuss the different types of RAM's bringing out their salient features. Give some idea of their speeds and relative costs. (10 Marks)
5. (a) Consider a processor system with 32 bit address capability, using 64 KB of cache, arranged to operate as a 4 way set associative cache. Work out the logic which determines cache hit or miss for this system. Assume you have 20-bit comparators available for the purpose. (10 Marks)
- (b) Describe the circuit and operation of a 4 bit carry look ahead adder. Compare the computational time, in terms of gate propagation times for a 32 bit adder using
i) 8 numbers of 4-bit carry look-ahead adders.
ii) 4 numbers of 8-bit carry look-ahead adders.
Assume no second level of look-ahead-carry generation. (10 Marks)
6. (a) Indicate the computational details of multiplying two 4-bit numbers 1011 and 0101 using Booth's algorithm. Verify the result obtained. (10 Marks)
- (b) Give the basic features of the IEEE floating point number standard. (10 Marks)
7. (a) Give the details of the system and the control signals for executing the following functions in a processor
i) *MOV R₁ to R₂*
ii) *LD M₁ to R₂ or ADD R₁ to R₂*. (10 Marks)
- (b) Give a brief out line of the sequence of actions produced by a processor to fetch and execute an unconditional branch instruction in terms of the specific control signals produced at each clock during the whole process. (10 Marks)
8. (a) Indicate the various steps in designing either the hardwired control for a microprocessor or microprogrammed control for a microprocessor. (10 Marks)
- (b) Describe the salient features of a simple microcontroller that can be embedded in systems like microwave ovens. (10 Marks)

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Reg. No. AVP03CS222

Fourth Semester B.E. Degree Examination, January/February 2006
Common to BM/EC/EE/TE/ML/IT/CS/IS
Computer Organisation

Time: 3 hrs.)

(Max.Marks : 100)

Note: 1. Answer any FIVE full questions.

2. All questions carry equal marks.

1. (a) Explain in brief the evolution of computer system. (6 Marks)
- (b) What is pipelining? How does it improve the performance? (8 Marks)
- (c) Write a short note on multiprocessor and multi computers. (6 Marks)
2. (a) Explain various types of rotate instructions (6 Marks)
- (b) Explain the features of RISC processor. (8 Marks)
- (c) Write the instruction format MOV AX CX instruction. (6 Marks)
3. (a) What are condition code flags? Explain the use of them. (6 Marks)
- (b) Explain basic instruction types with the help of examples. (4 Marks)
- (c) What is an addressing modes? Explain different types of addressing modes. (10 Marks)
4. (a) Draw and explain the timing diagram for modified synchronous input data transfer with multiple clock cycles. (6 Marks)
- (b) Which type of I/O devices are interfaced through DMA? Explain the bus-arbitration process used for DMA? (10 Marks)
- (c) Give comparison between memory mapped I/O and I/O mapped I/O. (4 Marks)
5. (a) Explain various types of SCSI bus termination. (5 Marks)
- (b) Explain the features of USB. (5 Marks)
- (c) Describe SDRAM and DDR SDRAM operations for data transfer between main memory and cache memory system. (10 Marks)
6. (a) In a two level virtual memory, $tA_1 = 10^{-7}$ and $tA_2 = 10^{-2}S$. What must be the hit ratio 'H' in order for the access efficiency to be atleast 90 percent of its maximum possible value. (5 Marks)

Contd. ... 2

- (b) Compare flash drives with hard disk drives. (5 Marks)
- (c) Draw the disk controller Interface connection and explain the major functions of disk controller. (10 Marks)
7. (a) Write a short note on look ahead carry generator. (5 Marks)
- (b) Explain how Booths algorithm is suitable for signed number multiplication in comparison of conventional shift and add method. (10 Marks)
- (c) Draw and explain typical hardwired control unit. (5 Marks)
8. (a) Draw and explain the multiple bus organisation. Explain its advantages. (10 Marks)
- (b) With a block diagram, explain the operation of a digital camera? (10 Marks)

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- 5 a. Draw a block diagram for $8m \times 32$ memory system using $512k \times 8$ memory chips and explain its operation. (08 Marks)
- b. Discuss direct mapped, associative mapped and set associative mapped CACHE memory system with suitable diagrams. (08 Marks)
- c. Define Hit Rate and Miss Penalty. (04 Marks)
- 6 a. Show the organization of a typical associative mapped TLB and explain how address truncation takes place. (10 Marks)
- b. Explain the organization and how data is accessed from a disk. State the typical values for recording surfaces, tracks, sectors, bytes / sectors, access time in a disk. (10 Marks)
- 7 a. Discuss the Booth's Multiplication Algorithm with an example. (10 Marks)
- b. With a clear diagram explain the floating point addition – subtraction unit. (10 Marks)
- 8 a. With a diagram which shows the separation Decoding and Encoding functions. Explain hard wired control (10 Marks)
- b. With a block diagram explain an embedded processor with all the salient blocks and their functions. (10 Marks)

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Fourth Semester B.E. Degree Examination, June / July 08
Computer Organisation

Time: 3 hrs.

Max. Marks:100

**Note : Answer FIVE full questions,
choosing at least two questions form each part. .**

PART – A

- 1
 - a. With a neat diagram explain different processor registers. (08 Marks)
 - b. Explain the important technological features and devices that characterized each generation of computers. (08 Marks)
 - c. Discuss two ways in which byte addresses are assigned. (04 Marks)
- 2
 - a. What is an addressing mode? Explain different generic addressing modes with an example for each. (08 Marks)
 - b. Define subroutine. Explain subroutine linkage using a link register. (06 Marks)
 - c. Explain the shift and rotate operations with examples. (06 Marks)
- 3
 - a. Explain the followings :
 - i) Interrupt concepts
 - ii) Interrupt hardware. (06 Marks)
 - b. Define exceptions. Explain two kinds of exceptions. (04 Marks)
 - c. What is the necessity of bus arbitration? Explain the different methods of bus arbitration. (08 Marks)
 - d. Define the following :
 - i) Cycle stealing
 - ii) Burst mode. (02 Marks)
- 4
 - a. Explain the important functions of input /output interface. (03 Marks)
 - b. With a neat block diagram, explain a general 8 bit parallel interface circuit.
 - c. Explain the followings with respect to USB. (08 Marks)
 - i) USB architecture
 - ii) USB addressing
 - iii) USB protocols. (09 Marks)

PART – A

- 5
 - a. With the block diagram, explain the operations of a 16 megabit DRAM configured as $2M \times 8$. (06 Marks)
 - b. Explain different mapping functions used in cache memory. (10 Marks)
 - c. What do you mean by memory inter leaving? Explain. (04 Marks)
- 6
 - a. What do you mean by address translation? Explain how TLB is used to implement virtual memory. (08 Marks)
 - b. Mention four major functions of disk controller on disk drive side. (04 Marks)
 - c. Explain how a 16 – bit carry look ahead adder can be built from 4 – bit adder. (08 Marks)
- 7
 - a. Show the multiplication of (+ 13) and (- 6) using multiplier bit pair recoding technique. (06 Marks)
 - b. Differentiate between restoring and non restoring division. (04 Marks)
 - c. Explain the IEEE standard for floating point number representation. (10 Marks)
- 8
 - a. Write and explain the control sequences for execution of following instruction.
Add (R3), R₁. (06 Marks)
 - b. With neat diagram, explain three bus organisation and write control sequence for the instruction
Add R₁, R₂, R₃. (08 Marks)
 - c. Differentiate between hardwired and micro programmed control. (06 Marks)



Fourth Semester B.E. Degree Examination, Dec.08 / Jan.09
Computer Organization

Time: 3 hrs.

Max. Marks:100

**Note : Answer FIVE full questions, selecting at least
two questions from each Part A and Part B.**

Part A

1. a. Explain the different functional units of a computer with a neat block diagram. (10 Marks)
b. Write the basic performance equation. Explain the role of each of the parameters in the equation on the performance of the computer. (05 Marks)
c. Represent the number 81234561 in 32-bit Big-endian and little-endian memory organization. (05 Marks)
2. a. What is the need for an addressing mode? Explain the following addressing modes with examples: immediate, direct, indirect, index, relative. (07 Marks)
b. What is subroutine linkage? How are parameters passed to subroutines? (06 Marks)
c. What is a stack frame? Explain. (07 Marks)
3. a. Discuss the different schemes available to disable and enable interrupts. (06 Marks)
b. How are simultaneous interrupt from more than one devices handled? (06 Marks)
c. What does the term "cycle stealing" mean? (02 Marks)
d. Write a note on any one bus arbitration scheme. (06 Marks)
4. a. Draw and explain the block diagram of a typical serial interface. How does it compare with a parallel interface? (10 Marks)
b. Explain the main phases involved in SCSI bus operation. (10 Marks)

Part B

5. a. Differentiate between SRAM and DRAM. (02 Marks)
b. Sketch and explain the internal organization of a $2M \times 8$ dynamic memory chip. (07 Marks)
c. Explain any one cache mapping function. (05 Marks)
d. A computer has byte addressable memory with a cache that can hold eight 32-bit words. Each cache block consists of one 32-bit word. The following sequence of hex addresses are read during program execution:
200, 204, 208, 20C, 2F4, 2F0, 200, 204, 218, 21C, 24C, 2F4
Assuming that the cache is initially empty, show the contents of the cache if
i) direct mapping is used ii) associative mapping with LRU replacement is used. (06 Marks)
6. a. Draw a block diagram and explain how a virtual address from the processor is translated into a physical address in the main memory. (05 Marks)
b. Write notes on: i) Optical technology used in CD systems ii) RAID Disk arrays. (08 Marks)
c. Draw a figure to illustrate and explain a 16-bit carry look ahead adder using 4-bit adder blocks. Show that the carry and sum are generated in 5 and 8 gate delays respectively. (07 Marks)
7. a. Draw the hardware implementation of Booth's multiplication algorithm. (04 Marks)
b. Trace the steps in the above implementation to multiply -5×-4 . (05 Marks)
c. Illustrate the steps for non-restoring division algorithm on the following data: dividend = 1011, divisor = 0101. (05 Marks)
d. If A and B are two single precision floating point numbers where
 $A = 44900000H$ and $B = 42A00000H$
Show the results of $(A+B)$ and $(A-B)$. (06 Marks)
8. a. Draw a figure of the single bus organization of the processor unit. (04 Marks)
b. List the actions needed to execute the instruction Add R1, (R3). Write the sequence of control steps to perform the actions for a single bus structure. Explain the steps. (10 Marks)
c. Compare hardwired control unit with micro programmed control unit. (06 Marks)

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06CS46

Fourth Semester B.E. Degree Examination, June-July 2009
Computer Organization

3

Time: 3 hrs.

Max. Marks:100

Note: Answer any FIVE full questions, selecting at least TWO questions from each part.

PART – A

- 1 a. Explain the function of processor registers with a block diagram. (08 Marks)
b. Write the basic performance equation. Explain the role of each of the parameters in the equation on the performance of the computer. (07 Marks)
c. Show how the operation $C = A + B$ can be implemented in a single accumulator computer by (i) Three-address instruction (ii) Two-address instruction (iii) One-address instruction (05 Marks)
- 2 a. What is an addressing mode? Explain register, indirect, index addressing modes with an example for each. (08 Marks)
b. What is subroutine linkage? Explain with an example, subroutine linkage using linkage register. (07 Marks)
c. Register R1 and R2 of computer contain the decimal value 1200 and 4600. What is the effective address of the source operand in each of the following instructions?
i) Load 20(R1), R5
ii) Move # 3000, R5
iii) Store R5, 30(R1, R2)
iv) Add -(R2), R5
v) Subtract (R1)+, R5 (05 Marks)
- 3 a. Explain with a diagram, how interrupt request from several I/O devices can be communicated to a processor through a single INTR line. (08 Marks).
b. How can the processor obtain the starting address of different interrupt-service routines using vectored interrupts? (04 Marks)
c. Why is bus arbitration required? Explain with block diagram bus arbitration using Daisy chain. (08 Marks)
- 4 a. Explain with a block diagram a general 8 bit parallel interface. (08 Marks)
b. With the help of data transfer signals explain how a read operation is performed using PCI bus. (08 Marks)
c. Explain briefly bus arbitration phase in SCSI bus. (04 Marks)

PART – B

- 5 a. Draw the organization of a $1K \times 1$ memory cell and explain its working. (08 Marks)
b. Explain the working of a single-transistor dynamic memory cell. (07 Marks)
c. Calculate the average access time experienced by a processor if a cache hit rate is 0.88, miss penalty is 0.015 milliseconds and cache access time is 10 microseconds. (05 Marks)

- 6 a. Show the organization of virtual memory address translation based in fixed-length pages and explain its working. (08 Marks)
- b. How can performance and reliability be improved using RAID technology? (04 Marks)
- c. Explain the design of a 4-bit carry-look ahead adder. (08 Marks)
- 7 a. Explain Booth's algorithm. Multiply 01110 (+14) and 11011 (-5) using Booth's multiplication. (10 Marks)
- b. Write the algorithm for binary division using restoring division method. (04 Marks)
- c. List the rules for addition, subtraction, multiplication and division of floating point numbers. (06 Marks)
- 8 a. Write and explain the control sequences for execution of an unconditional branch instruction. (10 Marks)
- b. Explain with block diagram the basic organization of a microprogrammed control unit. (08 Marks)
- c. What are the modifications required in the basic organization of a microprogrammed control unit to support conditional branching in the microprogram. (02 Marks)

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Fourth Semester B.E. Degree Examination, Dec.09/Jan.10

Computer Organization

Time: 3 hrs.

Max. Marks:100

Note: Answer any FIVE full questions, selecting at least TWO questions from each part.

PART - A

- 1 a. With a neat diagram, explain in detail the functional units of a computer. (10 Marks)
- b. How the performance of a computer is measured? Assuming that the reference computer is Ultra SPARCIO workstation with 300MHz Ultra SPARC-III processor. A company has to purchase 500 new computers, hence ordered testing of a new computer with SPEC2000 (run on reference as well as new computer). Following observations were made.

Programs	Runtime on reference computer	Runtime in new computer
1	50 Minutes	5 Minutes
2	75 Minutes	4 Minutes
3	60 Minutes	6 Minutes
4	30 Minutes	3 Minutes

The company's system manager will place the orders for purchasing new computers only if the overall SPEC rating is at least 12.00. After the said test, will the system manager place order for the purchase of new computers? (10 Marks)

- 2 a. Convert the following pairs of decimal numbers to 5 bit signed 2's complement binary numbers and add them. Also state whether overflow occurs in each case.
i) -5 & 7 ii) -3 & -8 iii) -10 & -13. (06 Marks)
- b. Write a program which evaluates the expression $A \times B + C \times D$ in a single accumulator processor. Assume that processor has load, store, multiply and add instructions and all the values fit in the accumulator. (05 Marks)
- c. Explain how the parameters are passed to a subroutine? Write a program to multiply a list of 'n' numbers stored in memory, which calls a subroutine namely, LISTMUL and trace the program with suitable example. (09 Marks)
- 3 a. In modern computers, why interrupts are required? Support your claim with a suitable example. (06 Marks)
- b. In the interrupt mechanism, how the simultaneous arrivals of interrupts from various (multiple) devices (I/O) are handled? (06 Marks)
- c. With neat sketches, explain the various approaches to bus arbitration. (08 Marks)
- 4 a. With a neat sketch, explain the individual input and output interface circuits. Also elicit their salient features. (10 Marks)
- b. In a computer system, why a PCI Bus is used? With a neat sketch, explain how the read operation is performed, along with the role of IRDY# / TRDY#, on the PCI Bus. (10 Marks)

Important Note: 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and/or equations written eg. 42+8=50, will be treated as malpractice.

PART – B

- 5 a. Draw a diagram and explain the working of a 16 mega bit DRAM chip configured as $2M \times 8$. Also explain as to how it can be made to work in fast page mode. (10 Marks)
- b. Assume that a computer has L1 and L2 caches. The cache blocks consist of 8 words. Assume that the hit rate is same for both caches and that it is equal to 0.95 for instructions and 0.90 for data. Assume also that the times needed to access an 8-word block in these caches are $C_1=1$ cycle and $C_2 = 10$ cycles, then answer the following:
- What is the average access time experienced by the processor if the main memory uses interleaving where the memory access parameters have usual meaning ($M=17$ with interleaving & $M=38$ without interleaving, assume that 30% of the instructions in a typical program perform a read or write operations). (04 Marks)
 - What is the average access time if the main memory is not interleaved? (04 Marks)
 - What is the improvement obtained through interleaving? (02 Marks)
- 6 a. Explain in detail, the working principle of a magnetic hard disk. (10 Marks)
- b. A disk unit has 24 recording surfaces. It has a total of 14,000 cylinders. There are an average of 400 sectors per track. Each sector contains 512 bytes of data. Answer the following questions.
- What is the maximum no. of gigabytes that can be stores in this unit? (04 Marks)
 - What is the data transfer rate in bytes/sec at a rotational speed of 7200 rpm? (03 Marks)
 - Using a 32-bit word, suggest a suitable scheme for specifying the disk address, assuming that there are 512 bytes/sector. (03 Marks)
- 7 a. Draw circuit diagram for binary division. Explain the restoring and non-restoring division algorithms with suitable examples. (10 Marks)
- b. Explain the concept of carry save addition for the multiplication operation, $M \times Q = P$ for 4-bit operands, with diagram & suitable example. (10 Marks)
- 8 a. Explain the process of fetching a word from memory using timing diagram of memory read operation. Also give an example for the same. (10 Marks)
- b. Write the control sequence of execution of the instruction ADD (R3), R1. For this sequence of instructions the processor is driven by a continuously running clock such that each control step is 2 ns in duration. How long will the processor have to wait in steps 2 & 5, assuming that a memory read operation takes 16 ns to complete? Also compute the percentage of time for which the processor is idle during the execution of this instruction. (10 Marks)

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Fourth Semester B.E. Degree Examination, May/June 2010
Computer Organization

Time: 3 hrs.

Max. Marks:100

**Note: Answer any FIVE full questions, selecting
at least TWO questions from each part.**

PART – A

- 1 a. PC contains the address of the instruction stored in main memory of the computer. The instruction is "MOVE (R3), R2". List the steps needed to execute the machine instruction MOVE (R3), R2. (08 Marks)
- b. Explain with examples, all the generic addressing modes, with assembler syntax. (12 Marks)
- 2 a. Convert the following pairs of signed decimal numbers to 5 bit 2's. Complement the numbers and add them. State whether overflow occurs or not.
i) -14 and 11 ii) -10 and -13 iii) -3 and -8. (06 Marks)
- b. What is word alignment of a machine (microprocessor based system)? Explain. What are the consecutive addresses of aligned words for 16, 32 and 64 bit word lengths of machines? Give two consecutive addresses for each case. (05 Marks)
- c. Bring out the five key differences between subroutine and interrupt service routine. (05 Marks)
- d. What is the function of an assembler directive? Give two examples of assembler directives used for the reservation of memory locations for variables. State their functions. (04 Marks)
- 3 a. Define and explain briefly the following:
i) interrupt.
ii) vectored interrupt.
iii) interrupt nesting.
iv) an exception and give two examples. (13 Marks)
- b. Explain in brief, with the help of a diagram, the working of daisy chain with multiple priority levels and multiple devices in each level. (07 Marks)
- 4 a. In a computer system, PCI bus is used to connect devices to the processor (system bus) bus. Consider a bus transaction in which the processor reads four 32-bit words from the memory. Explain the read operation on the PCI bus between memory and processor. Give signal and timing diagram. (12 Marks)
- b. Draw the block diagram of universal bus (USB) structure connected to the host computer. Briefly explain all fields of packets that are used for communication between a host and a device connected to an USB port. (08 Marks)

PART – B

- 5 a. Define and explain the following :
- i) Memory access time
 - ii) Memory cycle time
 - iii) Random access memory (RAM)
 - iv) Static memories. (04 Marks)
- b. Differentiate the static RAM (SRAM) and dynamic RAM (DRAM) giving four key differences. State the primary usage of SRAM and DRAM in contemporary computer systems. (04 Marks)
- c. Define memory latency and bandwidth in case of burst operation that is used for transferring a block of data to or from synchronous DRAM memory unit. (05 Marks)
- d. Draw a neat block diagram of memory hierarchy in a contemporary computer system. Also indicate relative variation of size, speed and cost per bit, in the hierarchy. (07 Marks)
- 6 a. Explain a simple method of translating virtual address of a program into physical address, with the help of a diagram. (08 Marks)
- b. Explain structural organization of moving head magnetic hard disk, with multiple surfaces for storage of data. Explain how moving head assembly works for reading data. (06 Marks)
- c. Answer the following with respect to the magnetic disk, the secondary storage device:
- i) seek time
 - ii) latency
 - iii) access time (06 Marks)
- 7 a. In carry – look ahead addition, explain generate G_i and propagate P_i functions for stage i with the help of Boolean expression for G_i and P_i . (04 Marks)
- b. Perform signed multiplication of numbers -12 and -11 using both multiplication algorithm. Represent the numbers in 5-bits including sign bit. Give booth multiplier recoding table that is used in the above multiplication. (08 Marks)
- c. Perform division of number 8 by 3 ($8 \div 3$) using non-restoring division algorithm. (08 Marks)
- 8 a. Draw the block diagram of the three-bus organization of data path, which provides multiple internal paths to enable several transfers to take place in parallel. Label the registers and functional components of the processor and their connection to the respective bus of data path. (16 Marks)
- b. Draw a block diagram of a complete processor and identify the units. (04 Marks)

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